REMARKS

Claims 1-20 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

The drawings were objected to under 37 CFR 1.83.

The Examiner alleges that the third transistor is not shown.

However, the Examiner's attention is directed to the instant Abstract where the third transistor is indicated as element 113.

Next, the Examiner's attention is directed to Figure 1 on the right hand side below elements 131 and 132 here, element 113 can be seen.

It is respectfully submitted that this is the third transistor and it is shown in the drawings.

Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

These rejections are respectfully traversed.

The Examiner alleges that to clamp after an ESD events is not fully clear and to delay during the ESD event is not clear.

The Examiner's attention is directed to Claim 1 where Claim 1 recites that the coupled clamp circuit and the delay circuit is operable to keep voltage at one or more

plurality of input nodes coupling the output of the delay circuit to a delay cell below a predetermined threshold.

This shows what is being clamped and delayed!

Furthermore, the Examiner alleges that it is unclear whether the data cell resided in line 2 is an additional limitation on the data cell as previously recited in Claim 1.

Applicants respectfully submit it is.

The remaining concerns are addressed by the amendment to Claim 6.

It is respectfully submitted that Claims 1-20 are in full compliance with 35 U.S.C. § 112, and particularly points out and distinctly claims the subject matter which Applicants believe is their invention.

Turning now to the art rejections, Claims 1-4 and 15-20 were rejected under 35 U.S.C. § 102 as being anticipated by Chang; and Claim 5 was rejected under 35 U.S.C. § 103 as being unpatentable over Chang.

These rejections are respectfully traversed.

It is respectfully submitted that Chang does not disclose or suggest the presently claimed invention including the delay circuit to delay during the ESD event as defined in independent Claims 1 and 18.

The Examiner alleges that elements 308 and 310 disclose a delay circuit to delay an output during an ESD device event.

However, the Examiner's attention is directed to column 11, lines 55-65 where Chang discloses that ESD protection circuits 306-1 and 306-2 serve as ESD clamps to protect transistors 308 and 310 from an ESD event, which could be caused by CDM.

If the ESD circuits are protecting transistors 308 and 310 from an ESD event they cannot delay during the ESD event.

Consequently, these elements cannot meet the requirements of the above mentioned claim language.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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